US006380559B1

(12) **United States Patent**
Park et al.

(10) **Patent No.: US 6,380,559 B1**
(45) **Date of Patent: Apr. 30, 2002**

(54) **THIN FILM TRANSISTOR ARRAY SUBSTRATE FOR A LIQUID CRYSTAL DISPLAY**

(75) Inventors: **Woon-Yong Park**, Kyungki-do; **Jong-Soo Yoon**, Choongcheongnam-do; **Chang-Oh Jeong**, Kyungki-do, all of (KR)

(73) Assignee: **Samsung Electronics Co., Ltd.**, Suwon (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 41 days.

(21) Appl. No.: **09/585,427**

(22) Filed: **Jun. 2, 2000**

(30) **Foreign Application Priority Data**

Jun. 3, 1999 (KR) 99-20515
Jul. 6, 1999 (KR) 99-27140
Jul. 8, 1999 (KR) 99-27548
Jul. 22, 1999 (KR) 99-29796

(51) **Int. Cl.**[7] **H01L 29/04**; G02F 1/136; G02F 1/1335

(52) **U.S. Cl.** **257/59**; 257/72; 349/106; 349/143; 349/158

(58) **Field of Search** 257/59, 72; 349/42, 349/43, 46, 106, 143, 147, 158

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,057,896 A * 5/2000 Rho et al. 349/42
6,087,678 A * 7/2000 Kim 257/59

* cited by examiner

Primary Examiner—Minh Loan Tran
(74) *Attorney, Agent, or Firm*—McGuireWoods LLP

(57) **ABSTRACT**

A thin film transistor substrate for a liquid crystal display includes an insulating substrate, and a gate line assembly formed on the substrate. The gate line assembly has a double-layered structure with a lower layer exhibiting good contact characteristics with respect to indium tin oxide, and an upper layer exhibiting low resistance characteristics. A gate insulating layer, a semiconductor layer, a contact layer, and first and second data line layers are sequentially deposited onto the substrate with the gate line assembly. The first and second data line layers are patterned to form a data line assembly, and the contact layer is etched through the pattern of the data line assembly such that the contact layer has the same pattern as the data line assembly. A passivation layer is deposited onto the data line assembly, and a photoresist pattern is formed on the passivation layer by using a mask of different light transmissties mainly at a display area and a peripheral area. The passivation layer and the underlying layers are etched through the photoresist pattern to form a semiconductor pattern and contact windows. A pixel electrode, a supplemental gate pad and a supplemental data pad are then formed of indium tin oxide or indium zinc oxide. The gate and data line assemblies may be formed with a single layered structure. A black matrix and a color filter may be formed at the structured substrate before forming the pixel electrode, and an opening portion may be formed between the pixel electrode and the data line to prevent possible short circuits.

17 Claims, 74 Drawing Sheets